GoldenEars ASIC Clock Configuration

## Clock Types:

This document describes how to configure the PLL clocks for the GoldenEars ASIC. There are three PLL clocks we are concerned with – CRM, CTM, and the CLM clock. All of these clocks are concerned with data transmission via the network PHY. In general the CLM clock is only used for CLEI mode. CRM and CTM are dependent on the type of PHY being used (MII, RMII, TBI etc)

## Setup Parameters and Constraints:

Each PLL channel generates a clock out based on the following formula:

F*out* = N/M \* F*in*

With the constraint that F*in*/M must be in the range of 10 to 100MHz

## CTM PLL:

The CTM PLL accepts an input frequency and generates the desired output for transmission. For the predefined Ethernet modes we are typically looking for 25MHz, 50MHz, or 125MHz clock rates. The CTM follows the above setup of F*ctm* = N/M \* F*in*

F*in* can be from any of the following:

* I\_REF\_CLOCK\_0 – which is 125MHz
* I\_REF\_CLOCK\_1 – which is 25MHz
* I\_SYS\_CLOCK – which is 24MHz
* The output of the CLM PLL (variable frequency)

N is a binary value that is written to bits [11:6] in the GRG\_PllConfig2 register

M is a binary value that is written to bits [5:0] in the GRG\_PllConfig2 register

**Note:** because of a quirk in the PLL hardware in the ASIC, the PLL must output twice the desired frequency (for example, in MII we want a 25MHz clock – we actually set the PLL to generate 50MHz). This doubled frequency is then divided out before being used by the PHY. This was done in order to introduce needed phase shifts in the wave forms. Any DDR style of PHY (RMII, RGMII, RTBI etc) needs the output phase shift to be 90 degrees, while any SDR style of PHY requires a phase shift of 180. (The phase shift is set in GRG\_PllConfig2 bits [21:20].)

### CTM Configuration Example: MII at 25MHz

1. Set GRG\_PllConfig bit [20] to b1 – Place the CTM in reset
2. Set GRG\_PllConfig bits [19:18] to b00 – Select 25MHz I\_REF\_CLK1 as the PLL input source
3. Set GRG\_PllConfig2 bits [21:20] to b00 (0x00) – Disable output (MII is synchronous)
4. Set GRG\_PllConfig2 bit [14] to b1 – sets the charge pump to 2X (recommended default)
5. Set GRG\_PllConfig2 bits [13:12] to b01 – PLL output will be in the range 50 to 100MHz
6. Set GRG\_PllConfig2 bits [11:6] to b000100 (0x04) – this is the N value described above
7. Set GRG\_PllConfig2 bits [5:0] to b000010 (0x02) – this is the M value described above
8. Set GRG\_PllConfig bit [20] to b0 – Release the CTM from reset
9. Poll GRG\_PllConfig bit [16] to ensure the PLL has locked

**Note:** bits [31:22] are unused/reserved. Bits [19:16] are individual phase shift settings – the recommended defaults for all of these are zero. Bit [15] is the PLL lock notification select – there are 2 options, the recommended default is also zero. See the general notes at the end of this document for more information.

## CRM PLL:

The CRM is the clock from the receive portion of the PHY. Setting it up is similar to the CTM, except you don’t have to specify an input source. As with the CTM, the PLL needs to generate 2X the clock rate for the phase shifting hardware to work. Again the PLL output is defined by N/M \* F*in*.

**Note:** For the CRM there is an option to insert a 1ns delay into the clock path. It is recommended to do this for all DDR type links (RMII, RTBI, etc). For SDR links (MII, GMII etc) do not enable this delay.

### CRM Configuration Example: RGMII at 125MHz

1. Set GRG\_PllConfig bit [12] to b1 – Place the CRM in reset
2. Set GRG\_PllConfig3 bit [22] to b1 – Insert 1ns delay into clock path (as described above)
3. Set GRG\_PllConfig3 bit [15] to b0 – Select default lock detection hardware
4. Set GRG\_PllConfig3 bit [14] to b1 – Set charge pump to 2X rate (recommended default)
5. Set GRG\_PllConfig3 bits [13:12] to b11 (0x03) – F*out* is between 200 and 400 MHz
6. Set GRG\_PllConfig3 bits [11:6] to b000100 (0x04) – this is the N term in the frequency calculation
7. Set GRG\_PllConfig3 bits [5:0] to b000010 (0x02) – this is the M term in the frequency calculation
8. Set GRG\_PllConfig bit [12] to b0 – Remove the CRM from reset
9. Poll GRG\_PllConfig bit [8] to ensure the PLL has locked

## CLM PLL:

The CLM PLL allows us to generate a wide range of clock frequencies. It’s intended for use with our custom CLEI link mode, and when in CLEI mode we feed the output of the CLM PLL into the CTM as its input. For the CLM the input is always the 60MHz USB PHY clock.

One key difference in the CLM setup is that there is an extra post-divider that will reduce the output frequency. The bit field for the post-divider can be set to zero (divide by 1) in order to disable it.

### CLM Setup Example: CLEI at 125MHz

This example is slightly more complicated, because we are configuring the CLM to generate one frequency, and then feeding that as the input to the CTM, which also needs to be configured. The first steps are to configure the CLM PLL:

1. Set GRG\_PllConfig bit [4] to 1 – Place the CLM in reset
2. Set GRG\_PllConfig4 bits [17:16] to b01 – Divide by 2
3. Set GRG\_PllConfig4 bit [15] to b0 – Select default PLL lock detection
4. Set GRG\_PllConfig4 bit [14] to b1 – Select 2X charge pump (recommended default)
5. Set GRG\_PllConfig4 bits [13:12] to b10 (0x02) – PLL out will be between 100 and 200MHz
6. Set GRG\_PllConfig4 bits [11:6] to b011001 (0x19) – this is the N multiplier for frequency
7. Set GRG\_PllConfig4 bits [5:0] to b000110 (0x06) – this is the M divider for frequency
8. Set GRG\_PllConfig bit [4] to 0 – Remove the CLM from reset
9. Poll GRG\_PllConfig bit [0] to ensure the PLL has locked

At this point the CLM is generating the 125MHz that will be our input to the CTM. The 125MHz is generated as follows:

F*in* (60MHz) \* [N(25)/M(6)] / Post Divider(2) = 125MHz

Configuring the CTM at this point is similar to the example above, but it is included for completeness.

1. Set GRG\_PllConfig bit [20] to b1 – Place the CTM in reset
2. Set GRG\_PllConfig bits [19:18] to b11 (0x03) – Select CLM PLL as the input source
3. Set GRG\_PllConfig2 bits [21:20] to b11 (0x03) – A phase shift of 180 degrees
4. Set GRG\_PllConfig2 bit [14] to b1 – sets the charge pump to 2X (recommended default)
5. Set GRG\_PllConfig2 bits [13:12] to b10 – PLL output will be in the range 100 to 200MHz
6. Set GRG\_PllConfig2 bits [11:6] to b000100 (0x04) – this is the N value
7. Set GRG\_PllConfig2 bits [5:0] to b000010 (0x02) – this is the M value
8. Set GRG\_PllConfig bit [20] to b0 – Release the CTM from reset
9. Poll GRG\_PllConfig bit [16] to ensure the PLL has locked

## General Notes:

The full discussion of the ASIC clocking scheme can be found at:

*U:\Projects\GoldenEars ASIC Standard Cell\90- Documents\90-01183 GoldenEars ASIC Clock Architecture*

The document above describes the operation in much greater detail, and is largely what this document is based on. It’s somewhat dense but covers all aspects of operation.

The specification for the Faraday PLL can be found at:

*U:\Projects\GoldenEars ASIC Standard Cell\90- Documents\90-01192 Goldenears Faraday 110nm ASICOverview*

This is the manufacturer of the PLL’s general specification, and has some useful information regarding the PLL operation and limits.